

## Professional Interests

Computer Architecture, Operating Systems, Very Large Data Sets, Asynchronous Systems, High Performance Computing, Quantitative Finance and Signal Processing

## Education

- Ph.D. Candidate in Computer Science - Expected October 2010  
University of Utah - Salt Lake City, UT.  
Advisors: Dr. Erik Brunvand, Dr. Rajeev Balasubramonian
- B.A. in Computer Science with High Honors - May 2002  
Colgate University - Hamilton, NY.  
Advisor: Dr. Chris Nevison

## Professional and Research Experience

- *FusionIO - External Research Liaison and Senior Software Engineer. Salt Lake City, UT. 2010 to Present*  
Engineer architecting next generation memory hierarchies based on high density non-volatile memories.
- *Common Futures Research - Owner. Salt Lake City, UT. 2003 to Present*  
Owner/Manager of a business that acquires, rehabs, and provides high quality, safe and secure living environments. Our focus group is families in the Salt Lake Valley area who might otherwise not be able to qualify for similar situations without assistance.
- *Univ. of Utah - Grad. Research Assistant. Salt Lake City, UT. 2002 to Present*  
Dissertation research focused on increasing operating system support in future chip multi-processors. Developing hardware innovations that can selectively isolate the OS from user execution at runtime, resulting in improved performance and power efficiency for server applications. Additional research into memory subsystem optimizations, memory controller interaction and policies, and cache coherence. Collaborative research with Huntsman Cancer Institute to determine relationship between DNA methylation and T-Cell leukemia via statistical datamining of the Danio Rero genome. See publications for specific research details. Advisors: Dr. Erik Brunvand, Dr. Rajeev Balasubramonian. Mentor: Dr. Kimble Frazer
- *Prediction Company - Systems Developer. Santa Fe, NM. 2006-2008*  
Developer creating systems that performed fully automated quantitative trading of US equities and treasuries. Work included bringing on-line a trading product for a new asset class including real time data collection, signal generation, order execution, and back end accounting. Developed a framework for automated data mining and back-testing potential signals using non-linear optimization. Worked with a small team including the CTO to rewrite both research and production data environments to allow high performance access to data sources exceeding 1TB in size. Mentor: Jim Nusbaum (CTO)
- *Intel Research - Grad. Research Intern. Hudson, MA. 2006*  
Researcher in Intel's FACT research group investigating the use of hardware performance counters to perform statistical analysis of hardware utilization. Real-time performance analysis is used to improve operating system scheduling algorithms for both performance and energy efficiency, as well as tracking the soft error rates of a microprocessor. Mentor: Dr. Athanasios Papathanasiou
- *Sun Microsystems Laboratories - Grad. Research Intern. Mountain View, CA. 2004*  
Researcher in Sun Labs' asynchronous circuits group investigating a novel computer architecture utilizing the GasP family of asynchronous control circuits. Investigation into using these circuits to form a high speed FLEET switching network as an on chip interconnect between microarchitectural structures. Work involved designing and simulating a latency tolerant, general purpose architecture that leveraged the advantages of an extremely fast switching interconnect. Microarchitecture focused on data movement, not computation, as the fundamental programming model. Mentor: Dr. Ivan Sutherland
- *Colgate University - Undergrad. Research Assistant. Hamilton, NY. 1999-2002*  
Researcher into areas of NP-Complete approximation algorithms, communicating sequential processes (CSP) over TCP/IP, and provably correct distributed computing algorithms. Advisor: Dr. Chris Nevison. Mentors: Dr. Laura Sanchis, Dr. Rod Moten

## Teaching Experience

- *University of Utah. Salt Lake City, UT. Fall 2009*  
Designed and taught a new special topics course with enrollment of 20 students, titled “Software Engineering For Very Large Data Sets”, and targeted at senior year undergraduates. Project based course covered the practical aspects of storing, accessing, and computing on data sets that are terabyte and larger in size. Topics included row vs. column oriented database models, distributed filesystems, and parallel programming across commodity clusters. Received hardware grants from Sun Microsystems and FusionIO for large database performance exploration as part of designing this course.
- *University of Utah. Salt Lake City, UT. Fall 2009*  
Guest lecturer for undergraduate course on C programming for non-majors.
- *University of Utah. Salt Lake City, UT. Spring 2009*  
Teaching assistant for advanced graduate course on memory system design.
- *University of Utah. Salt Lake City, UT. Fall 2002*  
Teaching assistant and guest lecturer for undergraduate computer architecture course.
- *Colgate University. Hamilton, NY. 1999-2002*  
Teaching assistant for seven different undergraduate computer science courses including introduction to programming, functional programming, computer architecture, set theory, and multiple advanced topics.
- *Tesuque Pueblo. Santa Fe, NM. Fall 2001*  
Taught a combined fifth and sixth grade class three days a week on basic computer proficiency.
- *Johns Hopkins Center for Talent Youth. Skidmore, NY. Summer 2001*  
Teaching assistant in both a classroom and laboratory setting instructing exceptional 13 to 16 year old students. Shared responsibility for planning and delivering college level computer science course material, assessing student progress, and judging future capabilities in computer science.
- *Colgate University Advanced Placement Computer Science Workshop. Hamilton, NY. Summer 2000*  
Teaching assistant at a week long summer workshop for high school teachers on the AP computer science curriculum. Helped teachers understand and be able to deliver effective instruction on a new case study to be used by the AP exam.

## Students Advised

- Joseph Kingston - Undergraduate researcher working in genomic statistical datamining. 2010

## Awards

- Best Paper Award Nominee - PACT, 2010
- U. Utah Research Opportunity for Undergrads (\$2,400), 2010
- Sun Microsystems University Teaching Grant - T5220 Server (Estimated Value: \$32,000), 2009
- FusionIO University Hardware Grant - 160GB IODrive (Estimated Value: \$7,500), 2009
- Colgate University Award for Excellence in Research, 2002
- Colgate University High Honors in Computer Science, 2002
- Colgate University Award for Outstanding Contribution to Computer Science, 2002
- Association for Computing Machinery (ACM) Syracuse Chapter, Four Year Award, 2001
- Upsilon Pi Epsilon National Undergraduate Computing Honor Society, 2001

## Service and Activities

- Technical reviewer for ASYNC '03-'05, HiPC '08-'09, PPOPP '10, ISCA '10, IEEE Transactions on Computers '09-'10
- Web chair for the 4th Workshop on Chip Multiprocessor Memory Systems and Interconnects (CMP-MSI), 2009
- Instructor at U. of Utah Alternative Energy Summer Camp for high school students, 2009
- Research Day Poster Competitions. U. of Utah, School of Computing. '05, '09-'10 (runner up both years)
- Santa Fe High School Varsity Soccer Coach, 2007
- Graduate student advisory committee. University of Utah, School of Computing, '03-'04
- Technology consultant for Santa Clara Pueblo Tribal Offices, 2001
- Member ACM, IEEE, SIGARCH, SIGMICRO

## References Available Upon Request

# Publications and Patents

---

## Refereed Conference Publications

- [1] SWEL: Hardware Cache Coherence Protocols to Map Shared Data onto Shared Caches - *PACT 2010*  
S. Pugsley, J. Spjut, **D. Nellans**, R. Balasubramonian
- [2] Handling the Problems and Opportunities Posed by Multiple On-Chip Memory Controllers - *PACT 2010*  
M. Awasthi, **D. Nellans**, K. Sudan, R. Balasubramonian  
*Best Paper Award Nominee*
- [3] Hardware Prediction of OS Run-Length For Fine-Grained Resource Customization - *ISPASS 2010*  
**D. Nellans**, K. Sudan, E. Brunvand, R. Balasubramonian
- [4] Micro-Pages: Increasing DRAM Efficiency with Locality-Aware Data Placement - *ASPLOS 2010*  
K. Sudan, N. Chatterjee, **D. Nellans**, M. Awasthi, R. Balasubramonian, A. Davis
- [5] A Case For Increased Operating System Support in Chip Multi-Processors - *IBM PAC<sup>2</sup> 2005*  
**D. Nellans**, R. Balasubramonian, E. Brunvand
- [6] ARCS: An Asynchronous Architectural Level Simulator - *GLSVLSI 2004*  
**D. Nellans**, V. Kadaru, E. Brunvand
- [7] Communicating Sequential Process In Java: Simplified Distributed Computing - *NCUR 2002*  
**D. Nellans**, C. Nevison
- [8] Algorithms For Finding Small Dominating Sets - *NCUR 2001*  
**D. Nellans**, L. Sanchis

## Refereed Journal Publications

- [1] Improving Server Performance on Multi-Cores via Selective Off-loading of OS Functionality - *LNCS 2010*  
**D. Nellans**, K. Sudan, E. Brunvand, R. Balasubramonian
- [2] OS Execution on Multi-Cores: Is Out-Sourcing Worthwhile? - *OSR 43:2 April, 2009*  
**D. Nellans**, R. Balasubramonian, E. Brunvand

## Refereed Workshop Publications

- [1] Improving Server Performance on Multi-Cores via Selective Off-loading of OS Functionality - *WIOSCA 2010*  
**D. Nellans**, K. Sudan, E. Brunvand, R. Balasubramonian  
*Extended version also appears as invited submission to LNCS 2010*

## Non-Refereed Publications

- [1] Interference Aware Cache Designs for Operating System Execution - *U. Utah Tech. Report UUCS-09-002 2009*  
**D. Nellans**, R. Balasubramonian, E. Brunvand  
*Portions of this work appear as WIOSCA 2010 and LNCS 2010*
- [2] BBCSP: A Distributed Branch and Bound Framework Within Java - *Colgate Univ. High Honors Thesis 2002*  
**D. Nellans**

## Patents

- [1] ABP: Predictor-Based Management of DRAM Row-Buffers - *USPO Prov. Patent Filed July 2010*  
**D. Nellans**, M. Awasthi, R. Balasubramonian, A. Davis